
**Optimizing power and performances
with STM32L4 series microcontrollers**

Introduction

Microcontrollers of the STM32L4 series are built using an innovative architecture to reach best-in-class, ultra-low power figures thanks to their high flexibility and advanced set of peripherals. The performance of the STM32L4 series blows away the competition in the ultra-low-power world by providing the best energy efficiency for applications.

STM32L4xx devices are based on Cortex[®]-M4 with FPU core. They can operate up to 80 MHz and achieve 100 DMIPS performances at 80 MHz, thanks to the integration of the ART Accelerator[™] while maintaining the smallest possible dynamic power consumption. The STM32L4 series feature the FlexPowerControl, which increases flexibility in power modes management while at the same time reducing overall application consumption.

In order to maximize battery usage and/or reduce its cost, the selection of the processor working mode is critical. In addition to power consumption considerations, application constraints also have to be taken into account. Consequently the microcontroller needs to offer a wide range of working modes in order to support all applications while always providing close to optimum power performance.

In many ultra-low power applications the microcontroller is used with long periods of sleep time followed by very short periods of dense processing.

This application note provides qualitative and quantitative information in order to be able to configure each operating point (frequency, range, low power mode..), before starting the implementation and optimization.

This application note uses the industry-standard ULPBench[™] benchmark from EEMBC as a reference case to correlate computations and simulations with measurements.

Related documents:

STM32L4 series core documentation and in particular:

- [1]. Reference manual: STM32L4x6 advanced ARM[®]-based 32-bit MCUs (RM0351)
- [2]. Application note: STM32L4 ultra-low-power features overview (AN 4621)
- [3]. STM32L476xx datasheet

Contents

- 1 Low-power application profile 5**
 - 1.1 Key parameters to consider 5
 - 1.2 ULPBench™ description 6

- 2 STM32L4 series low-power feature 7**
 - 2.1 Numerous low-power modes 7
 - 2.1.1 Low-power run and Low-power sleep modes 7
 - 2.1.2 Stop mode 8
 - 2.1.3 Standby mode 8
 - 2.1.4 Shutdown mode 8
 - 2.2 Run mode power consumption 9

- 3 Low-power mode selection methodology 11**
 - 3.1 PROCESS phase 12
 - 3.2 INACTIVE phase 12
 - 3.3 Sleep mode selection 13
 - 3.4 Run mode selection impact 14
 - 3.5 Impact of transition 15
 - 3.6 Impact of voltage and temperature 18
 - 3.7 Getting more accurate simulations 21

- 4 ULPBench™ use case optimization 24**
 - 4.1 Use case constraints 24
 - 4.2 PROCESS phase optimization 24
 - 4.3 INACTIVE phase optimization 24
 - 4.4 STM32L476xx measurements results 25
 - 4.5 Performance evolution with voltage range 26
 - 4.6 Peak current performances 27

- 5 Conclusion 28**

- 6 Revision history 29**

List of tables

Table 1.	Impact of wakeup energy on Standby	15
Table 2.	Impact of wakeup energy on Stop 2	15
Table 3.	Document revision history	29

List of figures

Figure 1. Application profile 5
Figure 2. Run modes current consumption 9
Figure 3. Run mode power efficiency 10
Figure 4. Application sequence and parameters 11
Figure 5. Influence of low-power mode on average current consumption 13
Figure 6. Influence of Run mode and frequency on average current consumption 14
Figure 7. Comparison Stop 2 versus Standby with SRAM2 16
Figure 8. Comparison Standby without SRAM2 retention versus Shutdown 17
Figure 9. Run mode correction with voltage and temperature 18
Figure 10. Low-power modes correction with VDD voltage 19
Figure 11. Low-power mode correction with temperature 20
Figure 12. Zoom on ULPBench™ sequence showing transitions 22
Figure 13. PCC simulation of ULPBench™ sequence 23
Figure 14. ULPBench™ measurements versus Run mode and frequency 25
Figure 15. Equivalent score as a function of supply voltage 26
Figure 16. ULPBench™ score versus peak current measurement 27

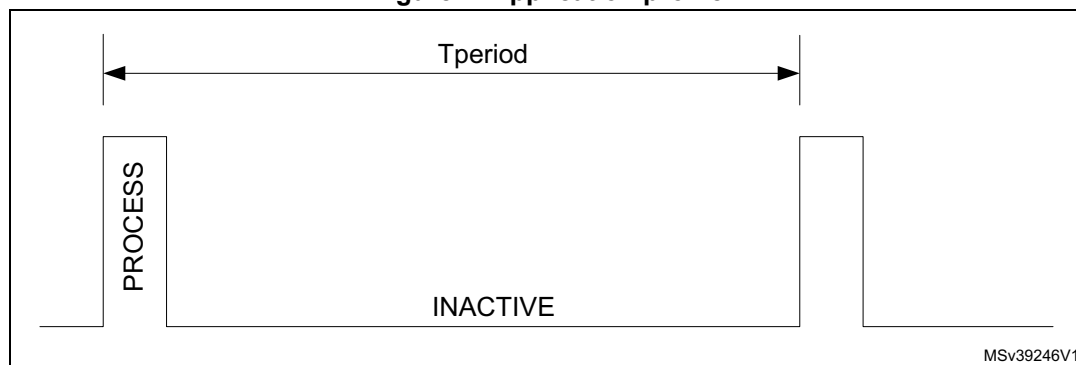
1 Low-power application profile

In applications where battery lifetime is a concern, the system must be optimized to provide maximum performance and reactivity at minimal power consumption.

This type of application contains generally two different phases:

- PROCESS phase, in which some sensor or radio information needs to be processed at either regular time intervals (RTC) or on external events (GPIO, interrupts..).
- INACTIVE phase, in which the system is sleeping and waiting for either RTC or GPIO wakeup.

Figure 1. Application profile



1.1 Key parameters to consider

Both phases have different performance criteria (in addition to power consumption):

- PROCESS phase requires a certain number of instructions to be executed in a given time frame.
- INACTIVE phase requires a certain minimal context to be kept (data RAM retention) and wakeup capability (peripheral, GPIO, RTC...) while keeping the power consumption as low as possible.

Furthermore, the transition between both phases must support different constraints:

- Sleep-to-Run transition requires a fast wakeup time with the smallest peak current (also called inrush current) at the time of transition, in order to allow the external supply to settle.
- Run-to-Sleep transition has less timing concerns, but needs to be optimized for energy saving.

When faced with such a bursty type of operation, four parameters need to be considered:

- Average power consumption. This parameter (P_{avg} expressed in μW) determines the battery size in order to support the expected autonomy.
- Maximum peak current. This parameter (I_{peak} expressed in μA) determines the type of battery that can be used but also the number and size of external components (decoupling capacitors) that need to be added on the board.
- Processing performances in PROCESS phase. This parameter is expressed in DMIPS which is proportional to the CPU frequency (Freq).
- Reaction time. This is the time between the activation of the wakeup signal source and the execution of the first instruction, generally within the interrupt service routine (ISR), once the context has been restored (Power, Data space context, clock..).

1.2 ULPBench™ description

The EEMBC ULPBench™ benchmark is well suited for evaluating ultra-low-power performances. It is a standardized test that allows characterization of any 8-, 16- and 32-bit microcontroller.

As of today, only the CoreProfile has been standardized. It allows evaluation of the following resources energy efficiency:

- CPU, RAM and Flash memory
- RTC timer and wakeup mechanism
- 32 kHz LSE
- Power management circuitry

During the PROCESS phase, the EEMBC ULPBench™ CoreProfile performs:

- data array manipulation including permutations and sorting
- simple filtering using 8 and 16-bit mathematics
- simple state machine
- simplified RTOS called TES, that allows to test real time events.

For comparing different microcontrollers, the ULPBench™ result is expressed as a score which is obtained by dividing 1000 by the average power consumption expressed in μW .

$$\text{Score} = \frac{1000}{\text{Avg_current} \times 3.0 \text{ V}}$$

where Avg_current (μA) is the current consumption I_{DD} measured at $V_{DD} = 3.0 \text{ V}$.

For more information on ULPBench™, please visit <http://www.eembc.org>.

In this application note the code runs from the Flash memory, regardless of its size.

2 STM32L4 series low-power feature

2.1 Numerous low-power modes

The microcontrollers of the STM32L4 series implement many different power modes, seven of them are low-power.

On top of these modes, the power consumption can be modulated by selecting different clock sources and Frequencies, as well as clocking off peripherals not in use.

In all these modes, except Shutdown, the safe power monitoring Brown out reset (BOR) and the IWDG can stay active to guarantee safe execution.

More details are provided in AN4621.

2.1.1 Low-power run and Low-power sleep modes

Two low-power active modes are available on the STM32L4 series in addition to those (Sleep, Stop and Standby) implemented on the STM32Fx series, they are the Low-power run and Low-power sleep.

They offer Run and Sleep mode functionality for applications with extremely low current consumption where some peripherals cannot be switched off, or where the CPU is processing continuously at low speed to minimize current variations.

Several features have been put in place to reduce the current consumption:

- the core logic is supplied by the low-power voltage regulator to reduce the quiescent current;
- the Flash memory can be switched off (power-down mode and clock gating) in Low-power sleep mode. It can also be switched off in Low-power run when the processor is executing from SRAM1 or SRAM2;
- the system clock is limited to 2 MHz maximum. The MSI internal RC oscillator can be selected as it supports several frequency ranges, with a small MCU total consumption down to 18 μ A in Low-power sleep Flash memory off at 100 kHz.

Batch acquisition sub-mode (BAM)

The STM32L4 microcontrollers support the power efficient batch acquisition sub-mode (BAM), in which data are transferred with communication peripherals, while the rest of the device is in low-power mode.

This is achieved by entering Sleep or Low-power sleep mode with this configuration:

- only the DMA, the communication peripheral(s) and the SRAM1 or SRAM2 clocks are enabled in Sleep (or Low-power sleep) mode;
- the Flash memory is off in Sleep (or Low-power sleep) mode: the Flash memory is in power-down and the Flash memory clock is gated off;
- if the system clock can be limited to 2 MHz, the main regulator is switched off (to enter Low-power sleep).

In Low-power sleep mode, the I2C and USART/LPUART peripherals can still be clocked with HSI at 16 MHz. This allows supporting BAM with I2C or USART at up to 1 Mbps speed.

2.1.2 Stop mode

The STM32L4 series implements two Stop modes with full SRAM and Peripheral retention capability and capacity to wakeup in 4 μ s thanks to the use of the MSI up to 48 MHz.

In these Stop modes all the high speed oscillators (HSE, MSI, HSI) are stopped, while the low speed ones (LSE, LSI) can be kept active. The peripherals can be set active, using the HSI clock when needed, to be able to wakeup the device on some specific events (such as UART character reception or I2C address recognition).

Stop2 mode implements a dedicated mechanism to keep the retention current as low as possible while allowing a very fast wakeup of 5 μ s from SRAM or 8 μ s from Flash memory.

2.1.3 Standby mode

In Standby mode the BOR is always enabled, ensuring that the device is under reset when the supply voltage is below the selected functional threshold.

By default the SRAMs content is lost in Standby mode. However, it is possible to preserve the content of the SRAM2 (with 230 nA additional consumption).

Pull-up and pull-down can individually be applied on each I/O during the Standby mode, allowing external devices configuration to be kept.

Wakeup from this mode is done thanks to one of the five wakeup pins, the reset pin or the independent watchdog. The RTC clocked by the low-speed oscillators (LSE or LSI) is also functional in this mode, with wakeup capability.

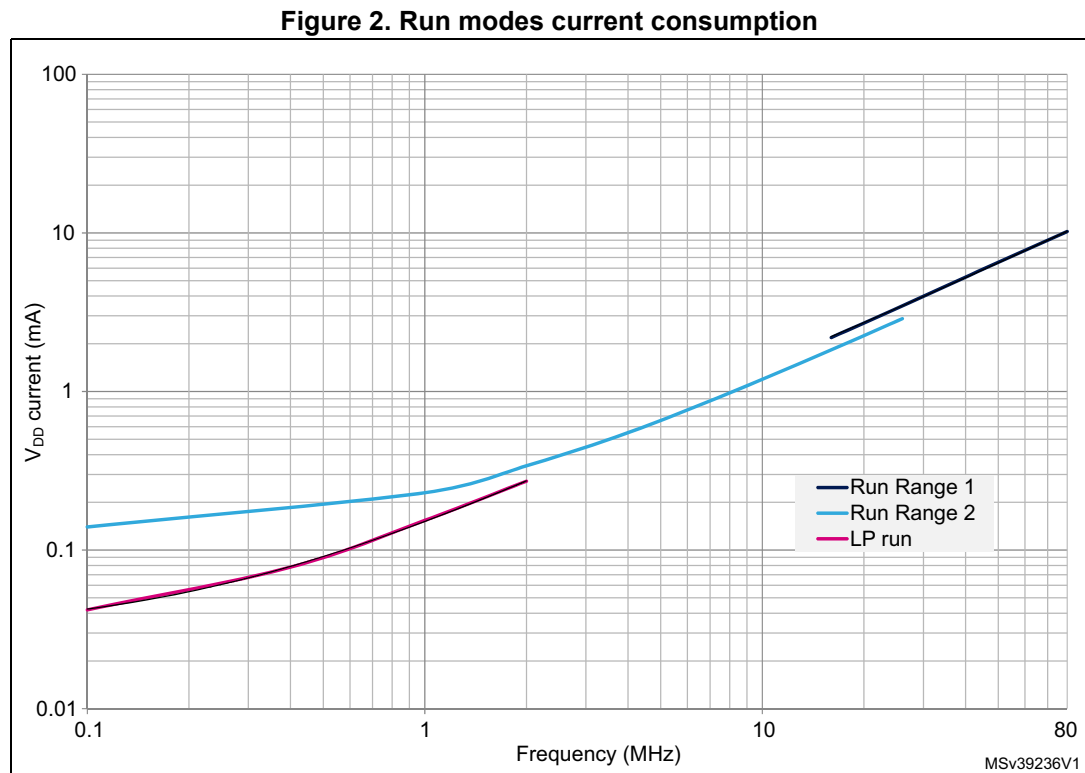
2.1.4 Shutdown mode

A new Shutdown mode is implemented in the STM32L4xx devices in order to lengthen even more the battery life of battery-powered applications.

This mode allows the lowest consumption (60 nA at 3 V), by switching off the internal voltage regulators, and by disabling the voltage power monitoring. Wakeup from this mode is done thanks to one of the five wakeup pins or to the reset pin. The RTC clocked by the low-speed external oscillator (LSE) is also functional in this mode, with wakeup capability.

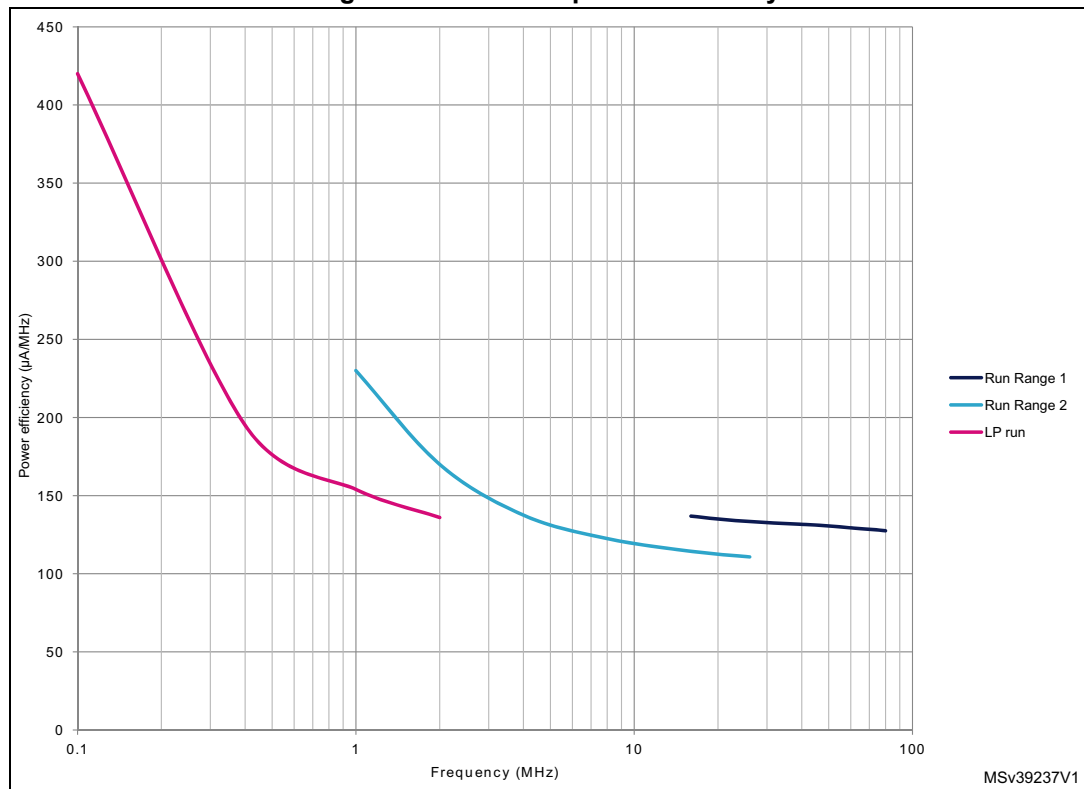
2.2 Run mode power consumption

Figure 2, extracted from [2], gives the typical current consumption values for the STM32L476 at 25 °C for different CPU frequencies while running the Fibonacci algorithm at 3.0 V supply:



This curve can be translated into power efficiency by dividing the current consumption, multiplied by V_{DD} to get power figure, by the CPU frequency, see Figure 3.

Figure 3. Run mode power efficiency



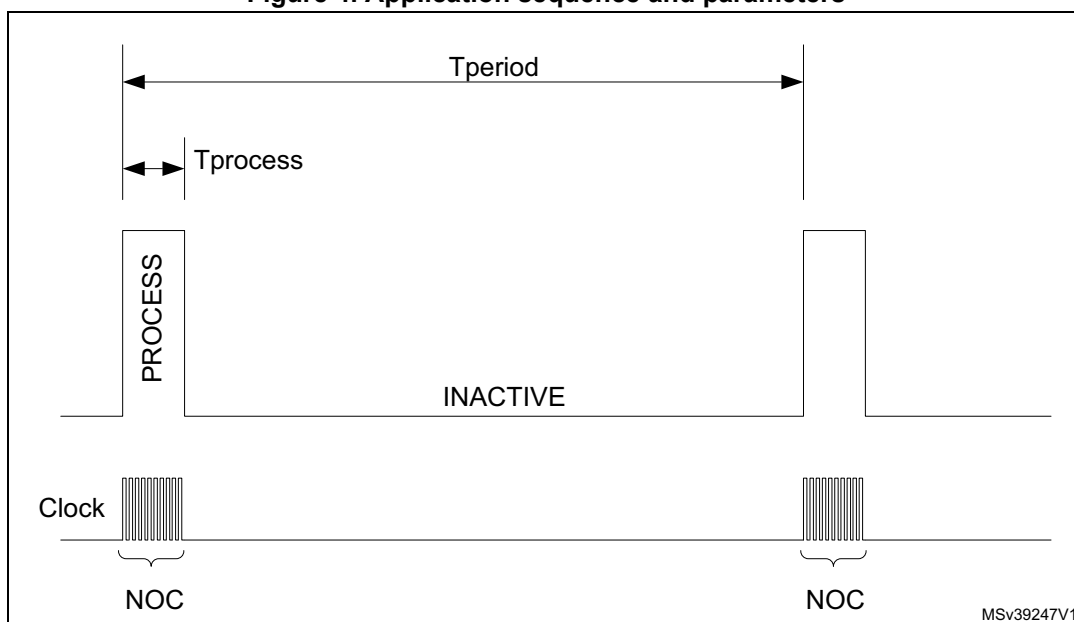
The optimum efficiency is obtained in Run Range 2 at the maximum frequency of 26 MHz.

3 Low-power mode selection methodology

We are considering a simplified application model where the application wakes up every Tperiod and performs some processing that is always the same and seen as a constant number of instructions (no waiting loops, no data dependencies). This allows us to make the following approximations:

- The PROCESS phase duration (Tprocess) can be defined in terms of the number of cycles (NOC) to be executed at each period. Defining F_{CLK} as the CPU System Clock frequency, the duration of the PROCESS phase is equal to Tprocess = NOC / F_{CLK}. The average current consumption during this phase is equal to Iprocess.
- The INACTIVE phase duration is Tperiod - Tprocess, and its average current consumption is inactive.

Figure 4. Application sequence and parameters



In order to get the average current consumption we have to sum-up both consumptions during the PROCESS phase and during the INACTIVE phase.

$$I_{average} = I_{process} \times \frac{T_{process}}{T_{period}} + I_{inactive} \times \frac{T_{period} - T_{process}}{T_{period}}$$

The PROCESS phase duration is proportional to the number of cycles to execute, which is a constant in our case:

$$I_{average} = I_{inactive} + (I_{process} - I_{inactive}) \times \frac{NOC}{F_{CLK} \times T_{period}}$$

The value NOC/(F_{CLK} × Tperiod) is usually called duty cycle.

This model does not take into account the consumption during the transition from INACTIVE to PROCESS phase which is addressed in [Section 3.5: Impact of transition](#).

Two parameters need to be selected to optimize the average power consumption:

- The Run mode and clock frequency that will be used during the PROCESS phase.
- The Low-power mode that will be used during the INACTIVE phase.

3.1 PROCESS phase

Depending on the processing requirement (DMIPS) we can use one of the different Run modes:

- Run1: Run mode with Range 1 voltage, with a maximum of 100 DMIPS when run at 80 MHz.
- Run2: Run mode with Range 2 voltage, with a maximum of 32.5 DMIPS when run at 26 MHz.
- LP run: Low-power run mode, with a maximum of 2.5 DMIPS when run at 2 MHz.

Another parameter that needs to be taken into consideration when selecting the frequency is the ability to support the constraints related to the peripherals, if any.

3.2 INACTIVE phase

The STM32L4 series provides different low-power modes that can be used for the INACTIVE phase:

- Sleep or low-power (LP) sleep
- Stop 1 (with regulator in low-power mode)
- Stop 2
- Standby (with RTC and SRAM2 retention)
- Shutdown (with RTC)

Depending on the source of wakeup and the duration of the sleep period, one of the following modes can be selected:

- Sleep or LP sleep: if the reactivity is the key parameter (in this case the wakeup time will only be 6 system clock cycles).
- Stop 1: if a lot of peripherals have to stay awake and the system has multiple sources of wakeup, including USB Suspend (in this case the application must tolerate a wakeup time from Flash memory of about 6.3 μ s).
- Stop 2: if few peripherals have to stay awake and can generate wakeup event as LPUART reception, LPTIM1 or I²C Slave Address recognition (in this case the application must tolerate a wakeup time from Flash memory of about 8.2 μ s).
- Standby: if no other peripherals than RTC need to stay awake, and up to 32 Kbyte of data retention is required (in this case the application must tolerate a wakeup time from Flash memory of about 14 μ s). Note that in this mode the LPUART and the I2C can wakeup the system quickly enough so that no loss of information occurs.
- Shutdown: if only the RTC and the backup registers need to stay awake (in this case the application must tolerate a wakeup time of about 256 μ s).

Note: Wakeup timing depends on the code location (Flash memory or SRAM1), the system clock sources and the frequencies, please refer to [3]. for detailed conditions. The above wakeup from Stop figures correspond to MSI at 24 MHz with the code in Flash memory.

3.3 Sleep mode selection

The following numerical results are based on typical specifications extracted from the STM32L476xx datasheet [3]. at 25 °C (typical value) with 32.768 kHz crystal LSE oscillator and RTC active all the time.

As shown in the previous section, the optimum power efficiency is obtained when using the Run Range 2 mode at 24 MHz (almost maximum frequency) using the MSI as source of clock.

Figure 5 gives the theoretical consumption, for different selections of low-power mode (Low-power sleep, Stop 1, Stop 2, Standby with RTC and SRAM2 retention, or Shutdown) with RTC in the INACTIVE phase, as a function of the average number of processing cycles needed in the PROCESS phase assuming a one-second wakeup cycle period.

Figure 5. Influence of low-power mode on average current consumption

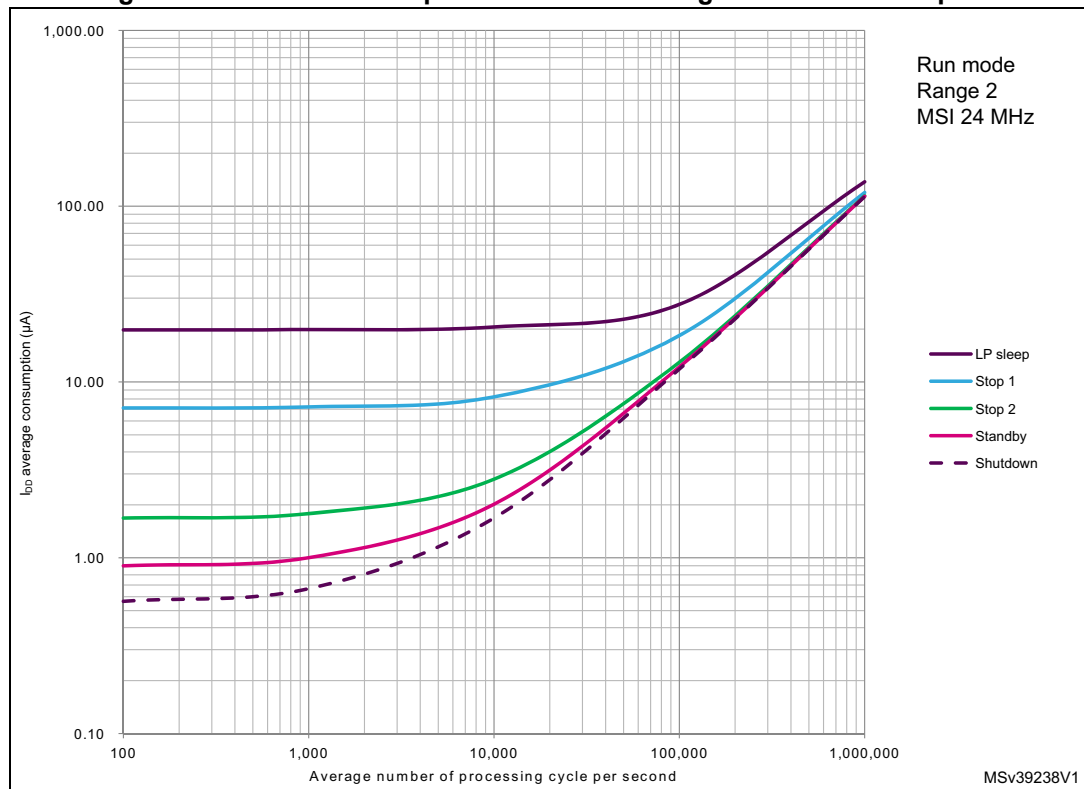


Figure 5 shows that, for applications requiring some data retention, the Standby low-power mode gives the best performance, whatever the number of cycles to be executed. It shows also that when the duty cycle increases (> 1Mega cycles per second), Stop 2 gives almost the same results as Standby.

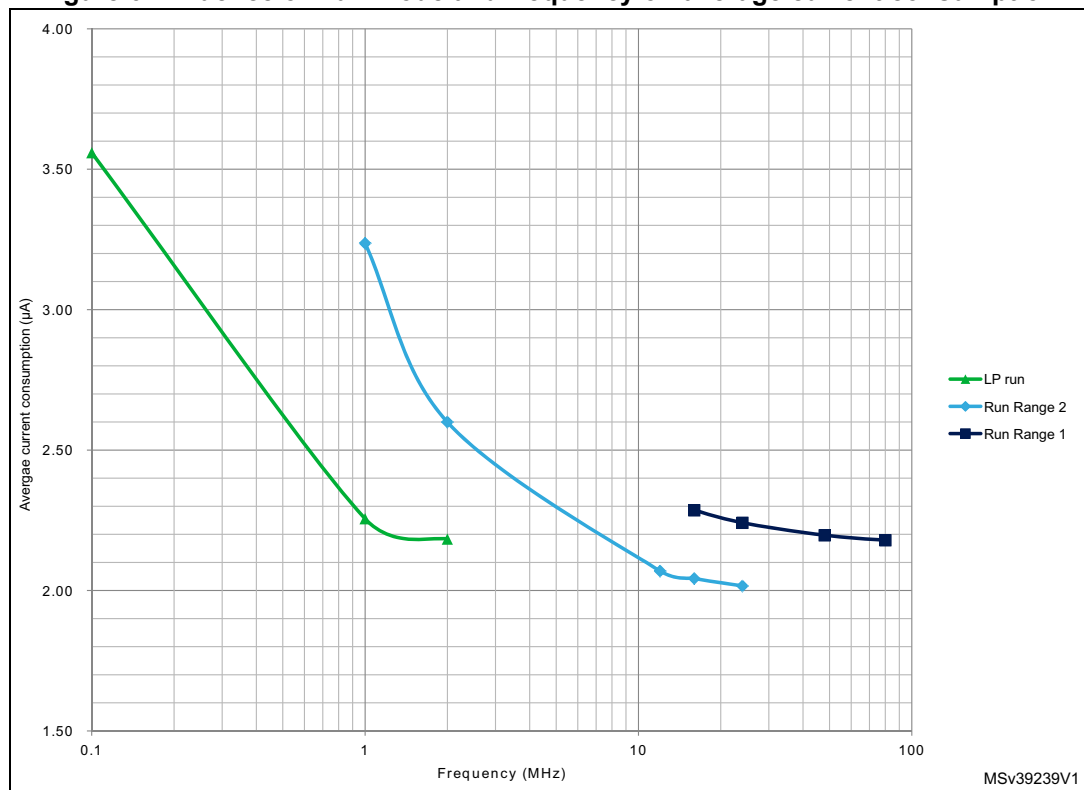
Shutdown mode has been discarded (dotted line) because it does not present enough data retention capability for this type of application.

However the choice of low-power mode is not only dictated by the overall power consumption figure, but also by other wakeup considerations linked to the application. [Figure 5](#) also shows that the STM32L4 series Stop 2 mode is very close to the Standby low-power mode while presenting a much more powerful and simpler setup for waking-up.

3.4 Run mode selection impact

When using Standby mode in the INACTIVE phase, [Figure 6](#) shows the influence of the Run mode used during the PROCESS phase on the average power consumption.

Figure 6. Influence of Run mode and frequency on average current consumption



[Figure 6](#) corresponds to 10 Kcycle of processing during the PROCESS phase. The three different segments correspond to the LP run (left part of the graph), the Run Range 2 (middle part) and the Run Range 1 (right part).

[Figure 6](#) confirms that the Run Range 2 at 26 MHz gives the best performance. However the STM32L4 series present very similar performances from 1 MHz up to 80 MHz, thanks to the three run modes. Simulations have been performed with other number of cycles (from 100 to 10M) giving the same optimum point.

3.5 Impact of transition

This study would be incomplete if it did not take into account the energy spent during the transition phases (wakeup and deactivation phases).

Thanks to its built-in capless regulators, the STM32L4 series needs a very low current to reload its internal nodes, once the voltage has been switched off and the device needs to wake up.

According to [3], at $V_{DD} = 3.0$ volts, the energy spent when leaving low-power mode is roughly:

- 32 nJ for transition from Stop 1 (with LPR) to Run Range 2.
- 50 nJ for a transition from Stop 2 to Run mode Range 2.
- 100 nJ for a transition from Standby to Run mode Range 1, with MSI at 4 MHz.
- 460 nJ for a transition from Shutdown to Run mode range 1.

In order to integrate the energy consumed during transitions into the overall consumption, we need to take into account the system wakeup period.

The tables below provide an estimation of the overall current consumption for both Stop 2 and Standby with SRAM2 in retention modes according to the Tperiod and the number of average cycles in the PROCESS phase.

Table 1. Impact of wakeup energy on Standby⁽¹⁾

-	Tperiod								
	1 ms	5 ms	10 ms	50 ms	100 ms	500 ms	1 s	5 s	10 s
Num cycle per sec.									
1000			4.40	1.68	1.34	1.07	1.03	1.01	1.00
10k	36.02	8.82	5.42	2.70	2.36	2.08	2.05	2.02	2.02
100k	46.17	18.97	15.57	12.85	12.51	12.24	12.21	12.18	12.17
1M	148	121	117	114	114	114	114	114	114
10M	1163	1135	1136	1133	1130	1129	1129	1129	1129

1. All values in μ A. Conditions: typical, 25 °C, 3.0 V.

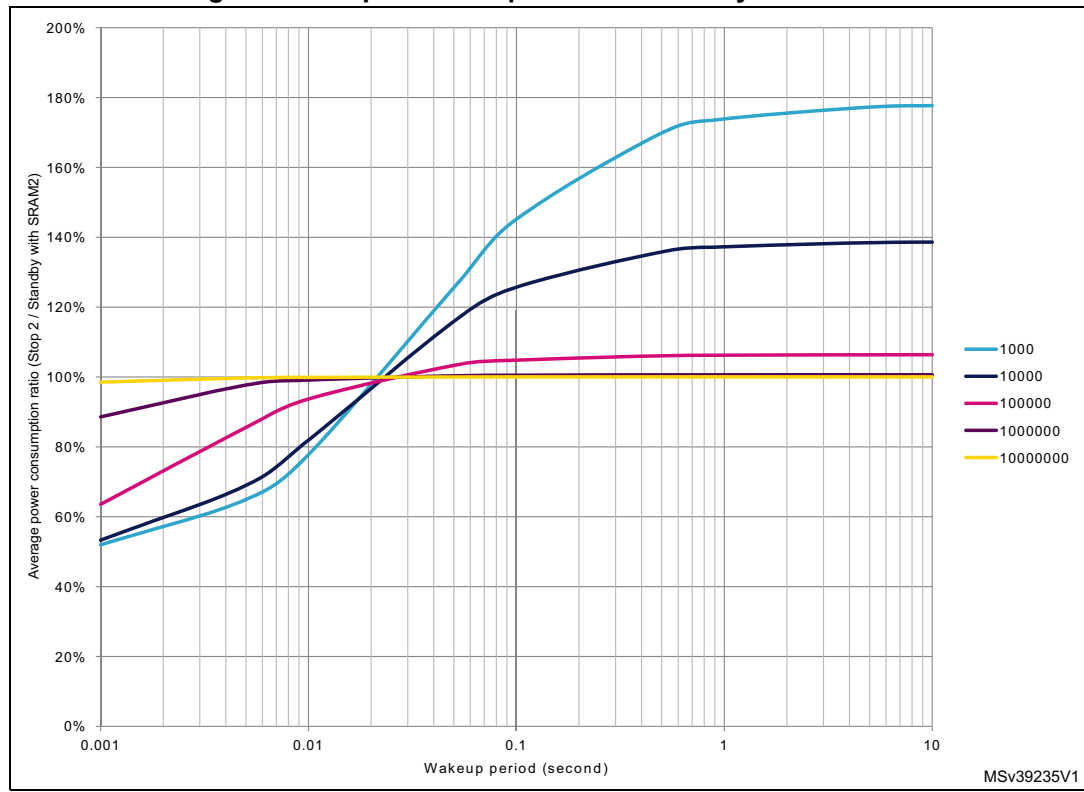
Table 2. Impact of wakeup energy on Stop 2⁽¹⁾

-	Tperiod								
	1 ms	5 ms	10 ms	50 ms	100 ms	500 ms	1 s	5 s	10 s
Num cycle per sec.									
1000			3.42	2.11	1.95	1.82	1.80	1.79	1.78
10k	19.20	6.08	4.44	3.13	2.96	2.83	2.81	2.80	2.80
100k	29.35	16.23	14.59	13.28	13.11	12.98	12.97	12.95	12.95
1M	131	118	116	115	115	114	114	114	114
10M	1146	1133	1131	1130	1130	1130	1130	1130	1130

1. all values in μ A. Conditions: typical, 25 °C, 3.0 V.

Figure 7 gives the ratio between Table 1 and Table 2:

Figure 7. Comparison Stop 2 versus Standby with SRAM2



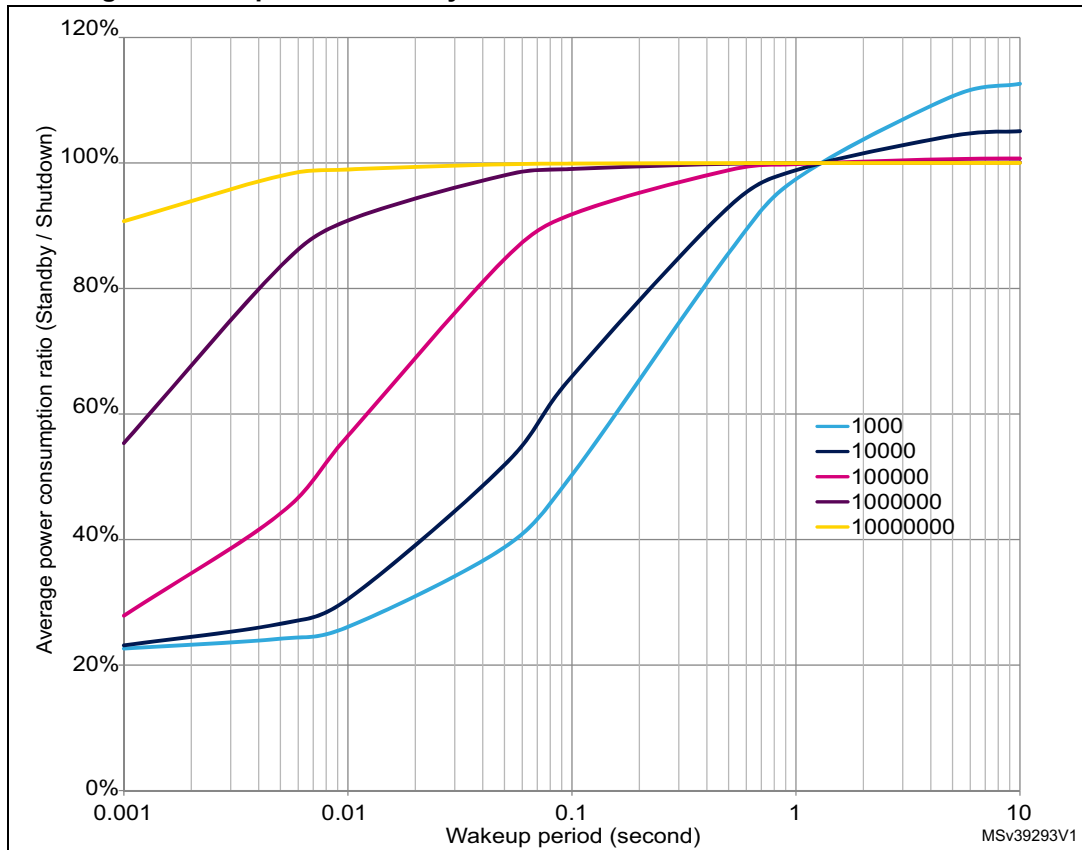
Note: When temperature increases the advantage provided by the Standby increases as well, for example the crossing point is 20 ms at 25 °C but become only 2 ms at 85 °C (and 70 ms at -20 °C).

The horizontal axis corresponds to the system wakeup period, the vertical axis corresponds to the ratio between the average consumption of the Stop 2 case and that of the Standby with SRAM2 case. The different curves, correspond to the number of cycles for the PROCESS phase.

If the wakeup period is below 20 ms Stop 2 is more interesting than Standby. If the number of cycles in the PROCESS phase is high (for example 1million and above) the interest of Standby decreases, as the consumption will be mainly driven by the Run mode used during the PROCESS phase.

Similar computation has been performed for Shutdown versus Standby, the crossing point is in the range of 2 seconds.

Figure 8. Comparison Standby without SRAM2 retention versus Shutdown



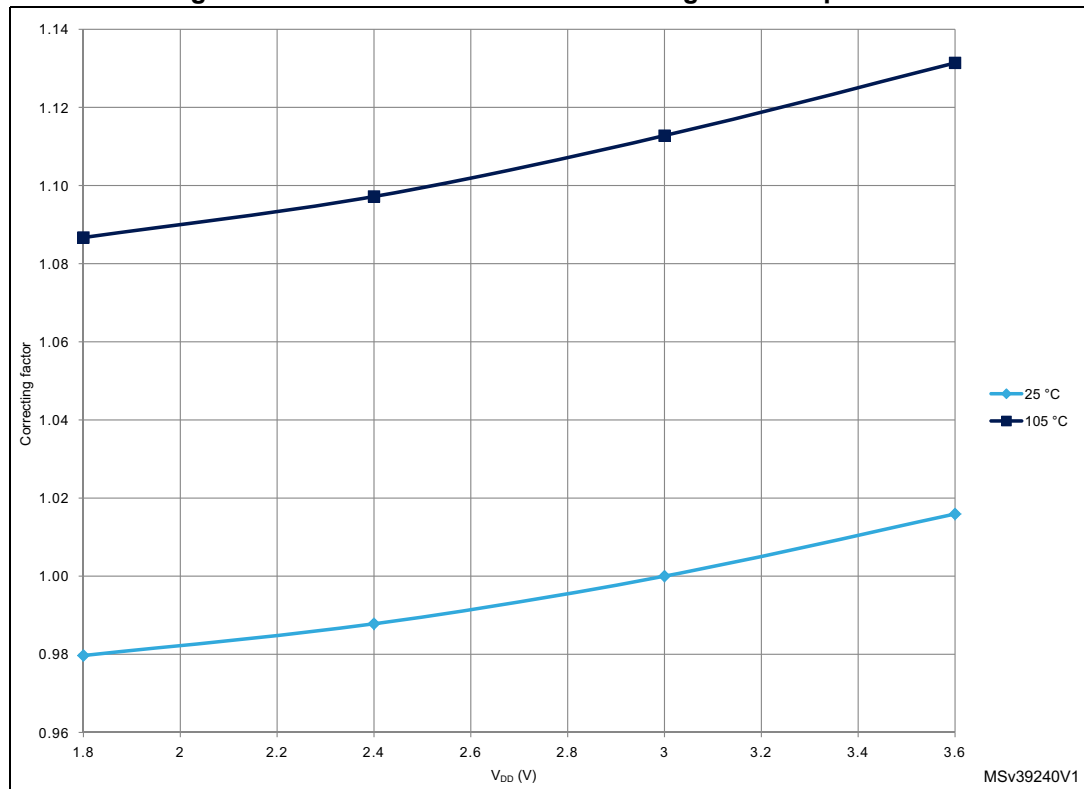
Note: In this theoretical study the number of instructions to reload the context is assumed to be taken into account in the PROCESS phase. In real implementation it will require more instructions to restart from Shutdown, Standby than STOP modes.

3.6 Impact of voltage and temperature

The previous data have been provided for $V_{DD} = 3.0\text{ V}$ and for a junction temperature of $25\text{ }^\circ\text{C}$.

The PROCESS phase current consumption varies very little with the voltage and the temperature. *Figure 9* gives the correction factor to apply for the Run Range 2 value at 24 MHz for varying V_{DD} voltage and temperature:

Figure 9. Run mode correction with voltage and temperature



The low-power modes have a stronger dependency on the voltage and temperature.

Figure 10 shows the correction factor to apply to the consumption for different low power modes and supply voltage:

Figure 10. Low-power modes correction with V_{DD} voltage

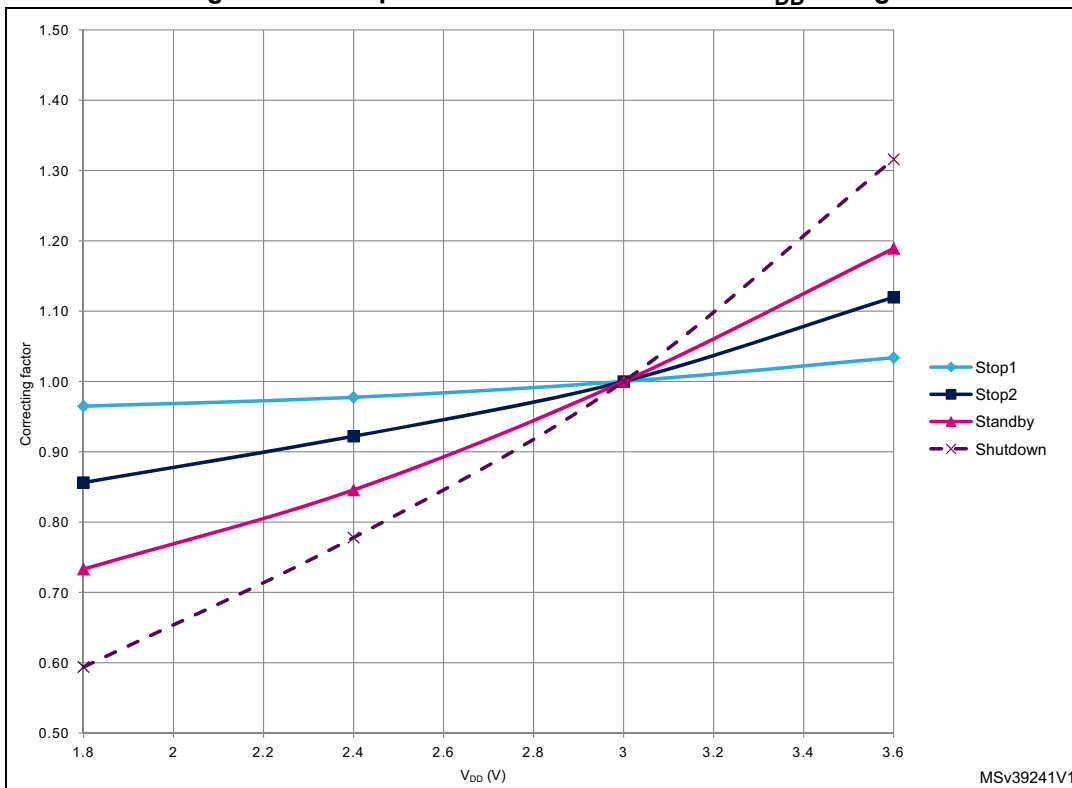
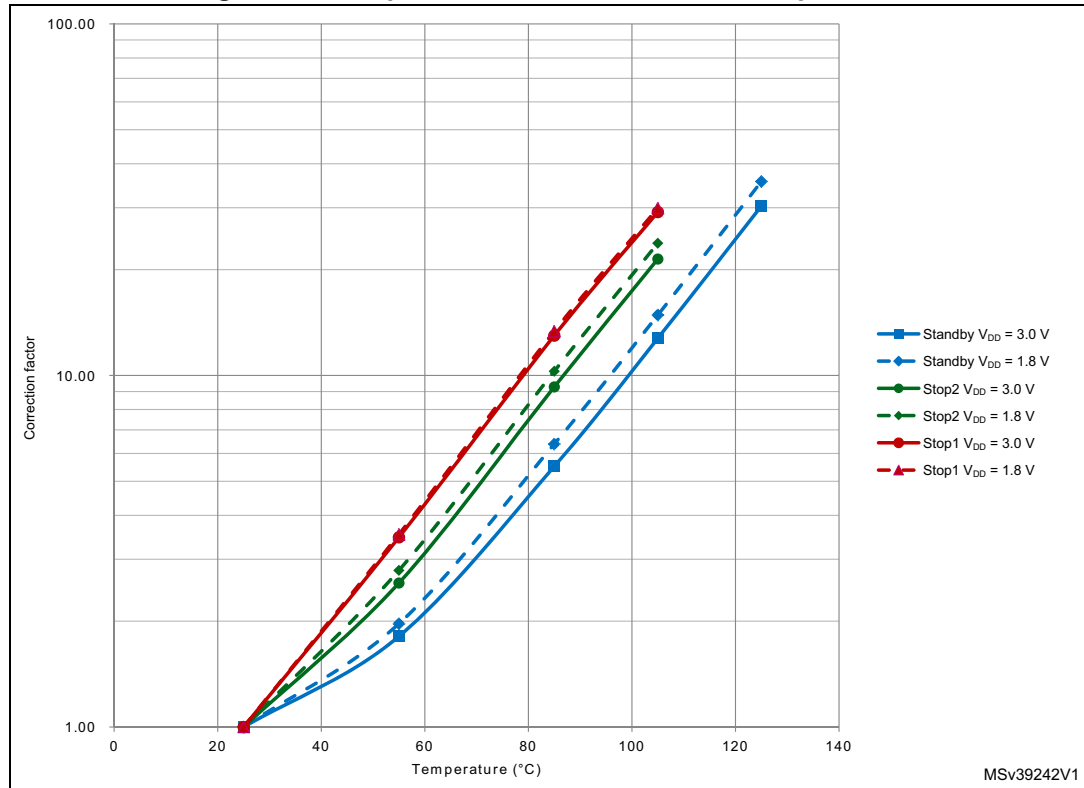


Figure 11 gives the correction factor to apply to the consumption for different low power modes and temperatures, for 1.8 V and 3.0 V supply:

Figure 11. Low-power mode correction with temperature



Above 45 °C, a good approximation is to consider that the low-power mode consumption doubles every 17 °C.

Similar theoretical optimization analysis has been performed over the whole range of temperature. The conclusion remains unchanged.

Reducing the voltage does not decrease significantly the current consumption in PROCESS phase (2 % gain for 1.8 V compared to 3.0 V). Nevertheless voltage reduction should be considered for following reasons:

- The INACTIVE phase current will be significantly lower (almost 30 % for Standby).
- As the power consumed by the system is the product of the current by the voltage, the power consumption will be at least 40 % lower (1.8 V versus 3.0 V).

In the example below the consumption in the PROCESS phase is 60 % of the overall consumption. If the voltage is reduced from 3.0 V to 1.8 V:

- the current consumption is reduced by 12 %
- the overall power consumption is reduced by 53 %.

3.7 Getting more accurate simulations

The approximation that the number of cycles (NOC) required to execute a task is constant with the CPU frequency is not exactly true. It tends to decrease when the CPU frequency decreases, because:

- The number of wait states required to access the Flash memory decreases when the frequency decreases
- The number of cycles spent by the processor in waiting loops decreases.

The number of processing cycles depends also on the low-power mode selection. It takes more instruction cycles to restore the context when using Standby mode with SRAM2 retention compared to other low-power modes.

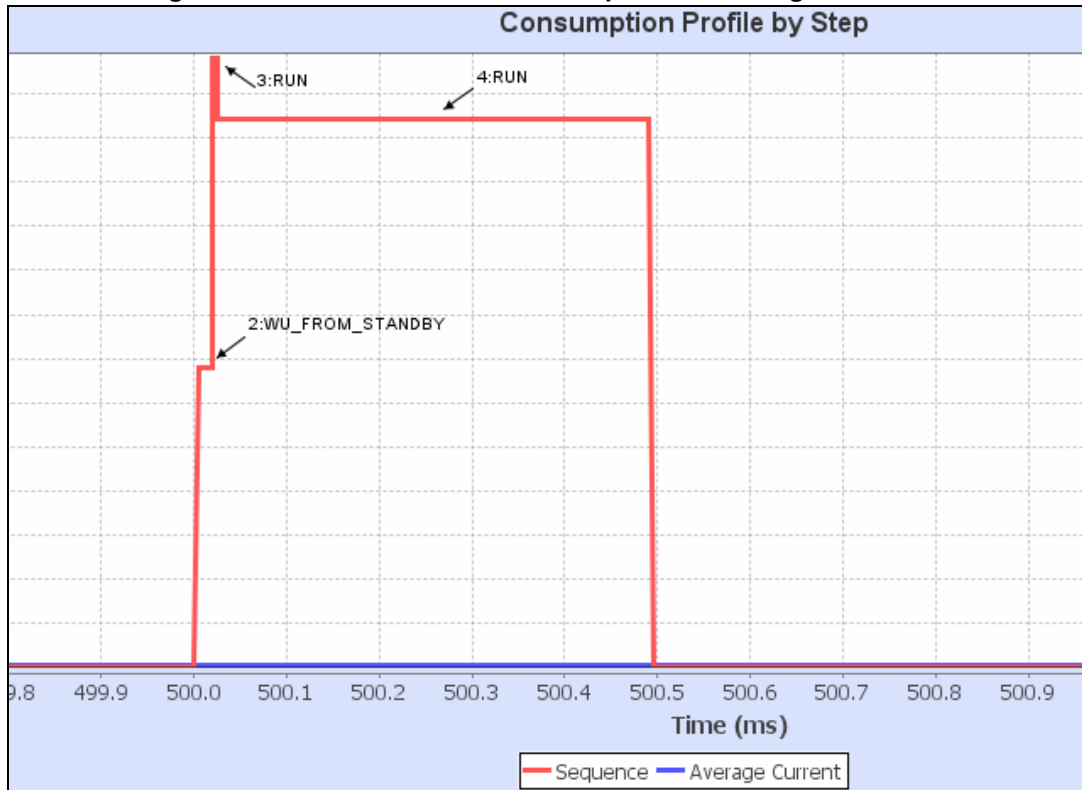
Finally the consumption required for the configuration of the peripherals during the active phase has also to be taken into consideration.

To help the customer to fine tune his application and make his own choices STMicroelectronics provides a Power Consumption Calculator (PCC) module within the STM32CubeMX that is available for free download from <http://www.st.com/stm32cube>.

PCC allows the average and peak power for a complex processing sequence to be computed accurately and helps with the selection of the appropriate modes according the different processing phases.

The following snapshots of the PCC tool screen correspond to a PROCESS phase of 10 K instructions, similar to the ULPBench™ sequence execution using Standby and Run Range 2 at 24 MHz. It allows us to take into account the transition from Standby to Run Range 1 then Run Range 2.

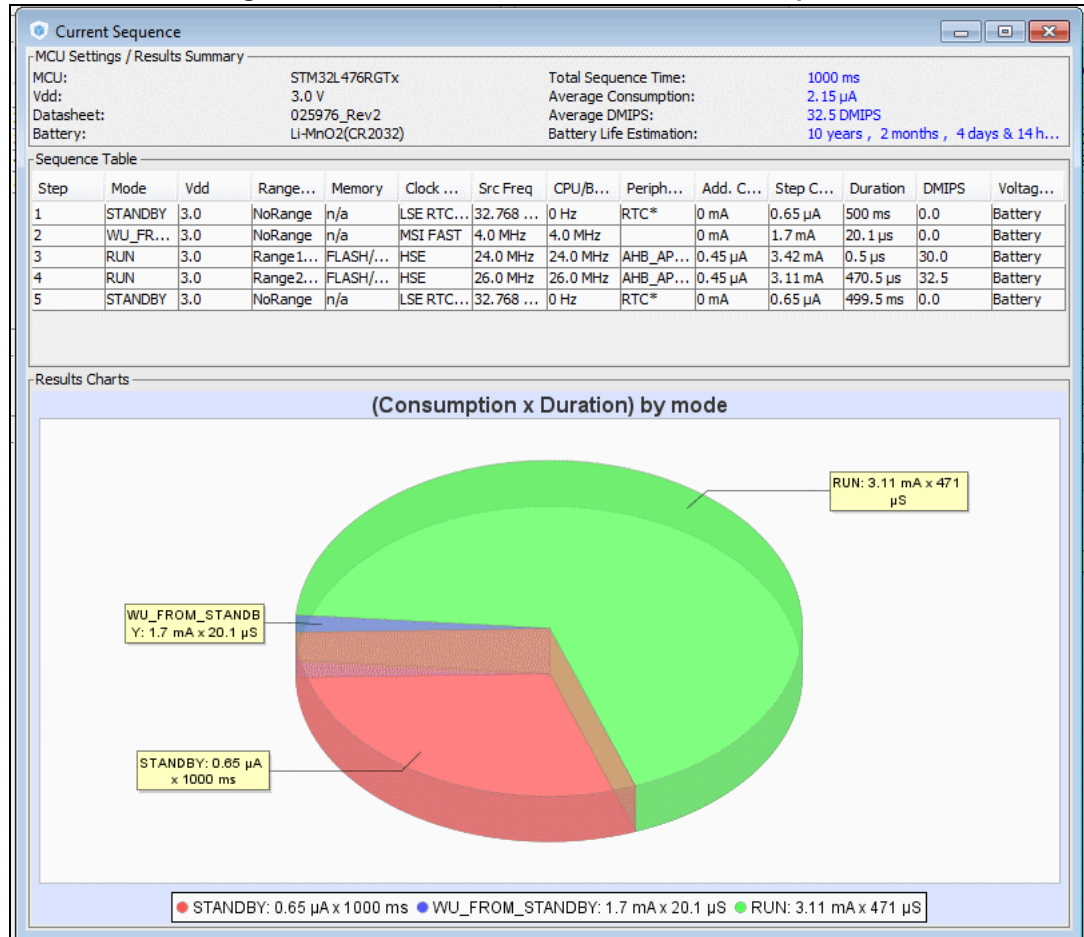
Figure 12. Zoom on ULPBench™ sequence showing transitions



The PCC tool interface provides:

- a table showing the configuration parameters for each processing step
- a chart showing the contribution of each phase to the overall power consumption.

Figure 13. PCC simulation of ULPBench™ sequence



4 ULPBench™ use case optimization

4.1 Use case constraints

The ULPBench™ imposes the following constraints:

- The application wakes up every second, based on an accurate RTC to perform some operations on a set of data.
- The data need to be maintained from one processing period to the next. This requires data retention during the INACTIVE phase.
- The amount of processing cycles required by the application, once compiled using the compiler strongest optimization option, is about 10000 cycles every second.

There are no particular constraints regarding reactivity of the system, in order to serve external events or the RTC periodic interrupts.

4.2 PROCESS phase optimization

Since the computation load is quite small (in the range of 10 Kcycle every second), any of the three Run modes can be used to execute the PROCESS phase within the one second time limit, down to a frequency of 10 kHz. In the same way, there is no particular limit on the maximum peak current that can be drawn and hence the maximum clock frequency that can be used.

Since there are no real-time aspect constraints (minimum latency to serve the ISR), we are not forced to select a very fast clock or wakeup time.

We can therefore use the power optimum point corresponding to the Run Range 2 at 24 MHz, using the internal MSI. When using the MSI at 24 MHz nominal frequency, it consumes less than any other solution using the PLL that would allow to reach the 26 MHz limit of the Run range 2.

Note: In the Range 2 mode, the efficiency figure is expected to be almost the same at 24 MHz, 16 MHz or even 12 MHz.

4.3 INACTIVE phase optimization

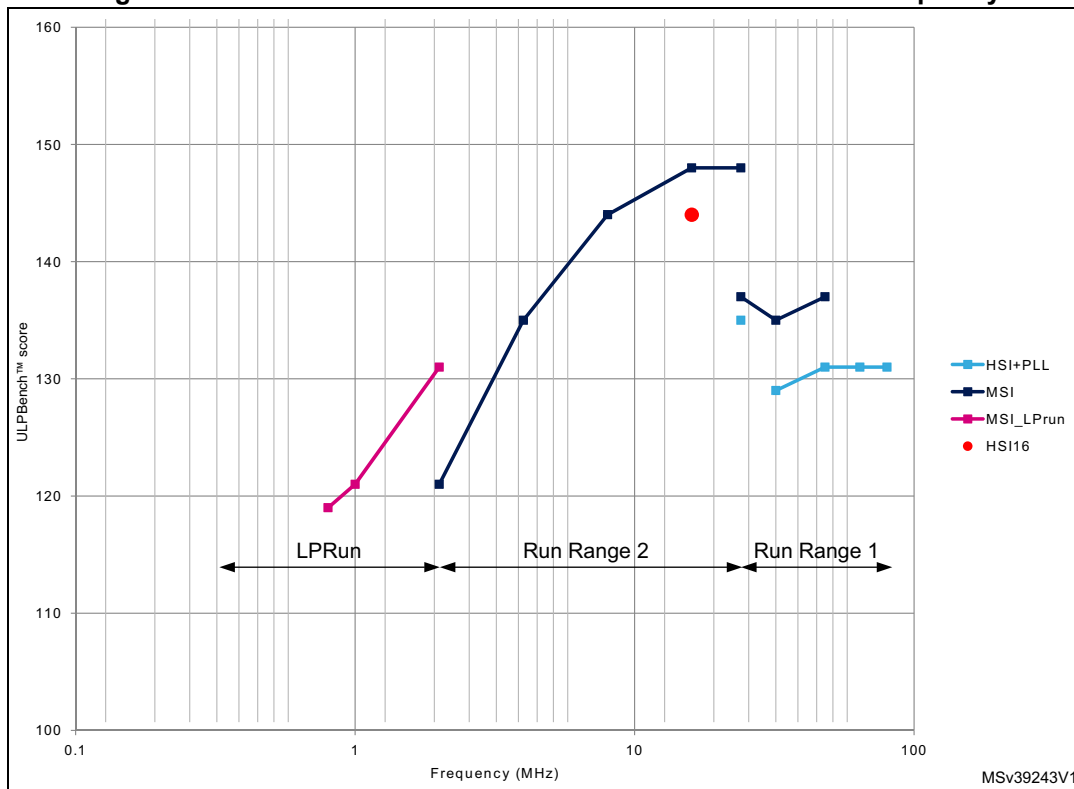
The ULPBench™ benchmark, requires to keep the data variables unchanged from one run to the next. Therefore the Shutdown mode cannot be used because it does not provide enough data retention capability for this application.

The most power efficient solution uses the Standby mode with RTC and retention in SRAM2.

4.4 STM32L476xx measurements results

Figure 14 gives the ULPBench™ score measurements depending on the Run mode and the system clock frequency used during the PROCESS phase. It uses the Standby mode with SRAM2 retention and RTC for the INACTIVE phase.

Figure 14. ULPBench™ measurements versus Run mode and frequency



The results are provided with different configurations of the clocks:

- For frequencies below 48 MHz, the MSI is used. This is because the MSI is automatically started when waking-up from Standby.
- For frequencies above 48 MHz, the HSI (at 16 MHz) and the PLL are used. Since we need to use the PLL and wait until it is locked, it is more interesting (better accuracy) to use the HSI at 16 MHz. In this case the MSI is stopped once the PLL has started.
- A special point using the HSI at 16 MHz is provided, without any PLL.

Note: For frequencies below or equal to 2 MHz, the LP run mode is used while for the range 2 MHz to 24 MHz, the Range 2 is used and for frequencies above 24 MHz the range 1 is used.

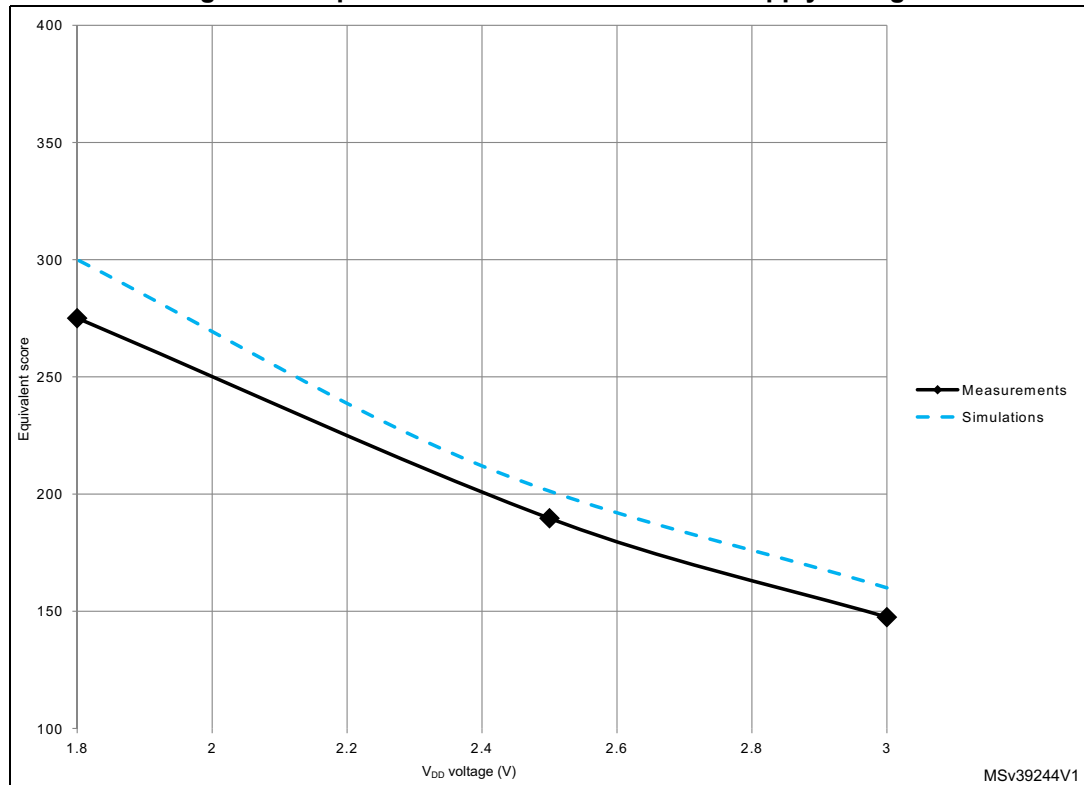
As already seen in the theoretical study, the Run Range 2 at 24 and 16 MHz, using the MSI provides the best results.

4.5 Performance evolution with voltage range

EEMBC has defined the ULPBench™ at 3.0 V only, however this voltage is not very representative of battery supplied low-power applications. As explained in the theoretical study, and unlike systems with DC/DC converters, the gain in power when moving to a lower voltage is very significant compared to staying at 3.0 V.

Figure 15 shows the ULPBench™ equivalent score measurement, calculated with the same formula at different voltages:

Figure 15. Equivalent score as a function of supply voltage



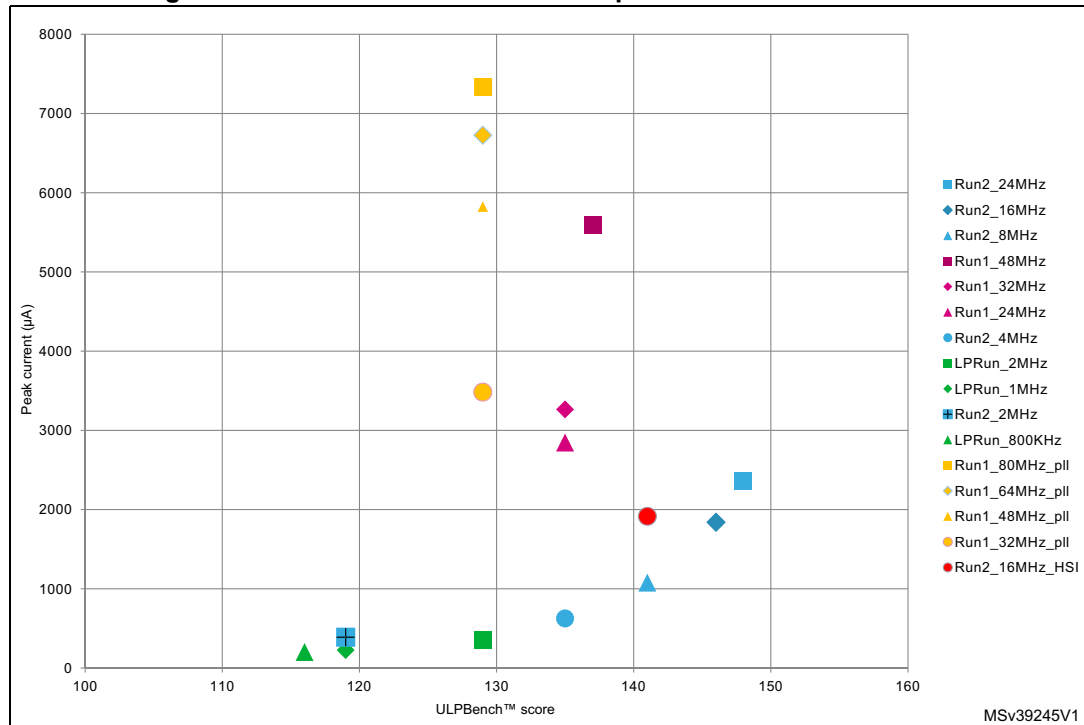
The above curve corresponds to the Run Range 2 at 24MHz MSI mode, it clearly shows the advantages of voltage reduction.

4.6 Peak current performances

This type of application, with very low average consumption, could present very high peak current. The higher the frequency, the higher the current peak. It can become the predominant parameter for the selection of the frequency and the operating mode used in the PROCESS phase.

Figure 16 shows the measurements of the peak current as a function of the ULPBench™ score.

Figure 16. ULPBench™ score versus peak current measurement



The above measurements have been performed on Nucleo-L476RG board assuming an impedance source of 200 Ω for frequencies below 48 MHz and 100 Ω for frequencies above. If the source impedance is lower, the peak current will increase up to the corresponding Run mode maximum.

Note: *The peak current drawn from the battery system depends a lot on the battery internal resistance as well as the decoupling capacitors placed on the PCB. Aged batteries or extreme temperature conditions could significantly increase this resistance, making the peak factor a decisive choice for the selection of the optimum mode.*

An easy way to reduce the peak current is to increase the input decoupling capacitance. On the Nucleo-L476RG board, in consideration of the PCB size and the bill of material, a maximum of 4.7 μF of tank capacitor can be used.

5 Conclusion

The STM32L4 series offers a large choice of options for optimizing both performance and power consumption, whatever the application.

This document provides guidelines based on experiments and quantitative results in order to help quickly selecting the best running modes and low-power modes, according to the characteristics and constraints of the end-user application.

In the case of the ULPBench™ benchmark^(a), with a wakeup period of 1 second and a processing load of about 10 Kcycle per period, the optimum choice is to use the Standby low-power mode for the INACTIVE phase associated with the Run Range 2 mode at 24 MHz (from the MSI) for the PROCESS phase. Other frequencies in the range 1 to 80 MHz give also very good results.

For a real application, the following rules apply, depending on the wakeup period:

- If the wakeup period is longer than some tens of ms an implementation using Standby provides better consumption.
- If the wakeup period is shorter, an implementation with Stop 2 will provide better results.
- If the temperature is high, the Standby mode should be preferred.

The selection of the low-power modes depends not only on the power consumption but also on the wakeup time requirement (system reactivity) and the requirement for data retention.

For STM32L4 series, if the processing can accommodate a frequency below 24 MHz, the optimum points are (in decreasing power efficiency order):

- Standby mode: if wakeup transition time can be longer than 20 μ s and retention area can be as small as 32 Kbyte.
- Stop 2: if wakeup transition time can be longer than 8 μ s and the application needs more than 32 Kbyte of retention

In the second case, the consumption penalty is less than 1.8 times the first case.

In any case, decreasing the V_{DD} voltage improves the power consumption significantly.

Ultimately if wakeup period is longer than a few seconds and retention memory is not needed, the Shutdown mode provides the best power performance. In this case the wakeup time is typically 256 μ s.

To help the customer to fine tune his application and make his own choice STMicroelectronics provides power consumption calculator (PCC) module within the STM32CubeMX that is available for free download from <http://www.st.com/stm32cube>.

a. This AN is using ULPBench™ results that have been improved since that time, please refer to the official score stored at <http://www.eembc.org> (search for ULPBench™).

6 Revision history

Table 3. Document revision history

Date	Revision	Changes
16-Sep-2015	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved